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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,274	03/24/2004	Kazutaka Akiyama	04173.0446	3986

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EXAMINER	
ANDUJAR, LEONARDO	

ART UNIT	PAPER NUMBER
2826	

MAIL DATE	DELIVERY MODE
04/16/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/807,274	AKIYAMA, KAZUTAKA	
	Examiner	Art Unit	
	Leonardo Andújar	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/17/2009*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,7,9,11,13 and 15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,7,9,11,13 and 15* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 12/11/2008 has been entered.

Priority

2. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Claim Rejections - 35 USC § 103

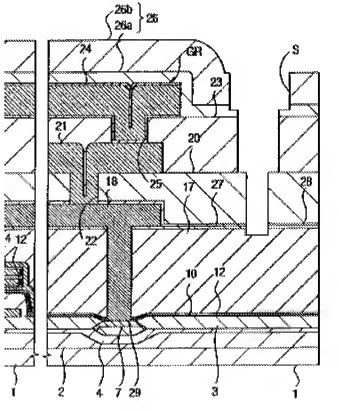
3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims1, 2, 7, 9, 11, 13 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suwanai et al. (US 5,994,762) in view of Wolf further in view of Kishida (US 6,770,977).

5. Regarding claims 1, 2, 13 and 15, Suwanai (e.g. fig. 11) shows a semiconductor device comprising: a semiconductor substrate 1; a first insulating film 17/27/28 formed above the semiconductor substrate and having a relative dielectric constant; a

conductor 18 (e.g. aluminum/tungsten, col. 2/lls. 5-11) which covers a side face of the first insulating film at least near four corners of the semiconductor substrate (note that 18 is part of a guard ring GR, see fig. 3), and a second insulating film 20 covering the outer side face of the conductor and having a relative dielectric constant of over 3.8 (inherent property of BPSG) wherein at least a part of the second insulating film (portion next to 18 and 28) being formed at a same distance from the semiconductor substrate as part of the first insulation film 28 to the semiconductor substrate as the first insulating film.



Suwanai does not teach that the first insulating layer has a relative dielectric constant of less than 3.8 nor a barrier layer on the at least an outer side face. Nevertheless, Wolf teaches that integrated circuits include a plurality of devices interconnected by multilevel interconnections including dielectric layers (pg 716-727). Also, the interconnect delay can be reduced by using low k dielectric material (e.g. nanoporous silica (SiO_2) "ultra low") having a dielectric constant of less than 2.0 (pgs. 791-795). Kishida (e.g. fig. 8b) teaches a barrier layer 202/203 composed tantalum nitride/tantalum is formed on an outer surface a conductor layer to prevent the metal atoms of the conductive layer from diffusing to the semiconductor substrate (col. 2/lls. 50-59 7 col. 8/lls. 26-28). It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a low k dielectric material (e.g. nanoporous silica SiO_2) having a dielectric constant of less than 2.0 for the first dielectric layer disclosed by Suwanai in order to reduce the interconnect delay as taught by Wolf and to include a barrier layer on an outer surface a conductor layer disclosed by Suwanai in view of Wolf to prevent the metal atoms of the conductive layer from diffusing into the semiconductor substrate.

6. Regarding claim 7, Suwanai shows that the second insulating film also covers an upper side of the first insulating film and a conductor 21 passing through the second insulating film positioned on the upper side of the first insulating film.

7. Regarding claim 9, Suwanai shows a conductive pattern buried in the first insulating film (e.g. 11, 15).

8. Regarding claim 11, Suwanai shows that the first insulating film is constituted of a plurality of layers 17/27.

Response to Arguments

9. Applicant's arguments filed 3/24/2009 have been fully considered but they are not persuasive. Applicant argues that the new added limitation is not taught by the prior art. However, Suwanai teaches that at least a part of the second insulating film being formed at a same distance from the semiconductor substrate as a part of the first insulation film (e.g. 28). Note that the part of first layer 28 and part of the second layer 20 have portions that are vertically parallel to each other; therefore part of second insulating film is formed at a same distance from the semiconductor such as any two points in an x axis sharing the same y coordinate. In other words, if an imaginary line is drawn in the x direction (horizontal) at a fixed y point that include 18, the line would intersect both of the layers at a common y distance. Thus, the prior art meets the claim.

Conclusion

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonardo Andújar whose telephone number is 571-272-1912. The examiner can normally be reached on Mon through Thu from 9:00 AM to 7:30 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sue Purvis can be reached on 571-272-1236. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Leonardo Andújar/
Primary Examiner, Art Unit 2826